REMARKS

Claims 1-17 are pending herein. In the Office Action, claims 9, 12 and 17 were objected to because of informalities, claims 7 and 9 were rejected under 35 U.S.C. §102(e) as being anticipated by US Pat. No. 6,496,038 to Sprague et al. (hereinafter "Sprague"), claims 12-17 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 6,191,618 to Gayles et al. (hereinafter "Gayles"), and claims 7-9 were rejected under 35 U.S.C. §103(a) as being unpatentable over US Pat. No. 6,650,145 to Ngo et al. (hereinafter "Ngo") in view of Sprague.

Claims 1-6 were allowed. Claims 10 and 11 were objected to as being dependent upon a rejected base claim, but were otherwise considered allowable.

Claim 9 was objected to since the recitation "low" regarding the state of the first node in the last "wherein" clause should instead be changed to --high--. In this case, the phrase "is pulled low" is replaced with --remains high-- in response to the clock signal going high since the first node is already pre-charged high when the clock signal is low. Applicant requests approval of this amendment and withdrawal of this objection to claim 9.

Claim 12 was objected to since the recitation "as" in the second to last clause "driving a third node to an opposite logic state *as* the second node" (emphasis added) should be changed to --of-- in order to particularly point out and distinctly claim the subject matter. Claim 12 is amended in accordance with that stated in the Office Action. Applicant requests approval of this amendment and withdrawal of this objection to claim 12.

Claim 17 was objected to since the recitation "second" in the second clause "pulling the output node low if the first and *second* nodes are both high" (emphasis added) should be changed to --third--. Claim 17 is amended in accordance with that stated in the Office Action. Applicant requests approval of this amendment and withdrawal of this objection to claim 12.

Applicant respectfully traverses the §102(e) rejection of claims 7 and 9 as being anticipated by Sprague.

Sprague does not show a keeper circuit coupled to a second node that drives a third node to an inverted logic state as the second node as recited in claim 7. The devices 265 and 260 shown in Sprague form a keeper circuit. In the Office Action, the static stage 230A is artificially included as part of the keeper circuit in an attempt to meet the claim language in order to drive a separate node. Yet the static stage 230A is part of the static logic 230 that is within a static environment which is separate from the pulsed environment. The keeper circuit elements 265 and 260 are part of a latch 220 which "provides a static signal from a pulsed input signal and acts as an interface between pulsed and static environments" (Sprague col. 5, lines 65-67), where the static stage 230A is the first stage of the static environment.

And further, Sprague does not show an output circuit coupled to first and third nodes which drives an output node high if the first or third nodes are low and that drives the output node low if the first and third nodes are both high as recited in claim 7. It is clear from the claim language that the output circuit in claim 7 is coupled to *both* the first and third nodes and responsive to the collective states of both of the first and third nodes

to drive the proper state of the output node. In Sprague, the static stages 230B-230D are coupled in series and the first stage, 230B, is not coupled to the first node but is only coupled to, and thus only responsive to the state of, the output of the first static stage 230A.

It is noted that the embodiment of FIG. 2 of Sprague is closer in configuration and function to the traditional inverting domino register 100 shown in FIG. 1A as described in Applicant's application starting with paragraph 6 on page 3. As described in paragraph 11 beginning on page 6 of Applicant's disclosure as filed, in order to provide the appropriate output interface and a non-inverting state, designers had to add additional logic stages (e.g., inverter 115) resulting in "disadvantageous consequences", such as, for example, the added delay of the added logic stage(s). The static logic 230 shown is Sprague is configured as a set of series-coupled static stages, which results in the same disadvantageous consequences and added delay as described in Applicant's disclosure. A non-inverting domino register according to an embodiment of the present invention has a faster data-to-output time than conventional approaches without compromising the stability of the output.

Claim 7 is amended, solely for purposes of clarity, to recite that the output circuit has a first input coupled to the first node, a second input coupled to the third node and an output coupled to the output node. Applicant respectfully submits that Sprague does not show a register including an output circuit having a first input coupled to a first node, a second input coupled to a third node and an output that drives the output node high if the first or third nodes are low and that drives the output node low if the first and third nodes are both high as recited in claim 7. Applicant respectfully asserts that claim 7 is

allowable over Sprague and that claim 9 is allowable as depending upon allowable claim 7. Applicant request withdrawal of this rejection.

Applicant respectfully traverses the §102(b) rejection of claims 12-17 as being anticipated by Gayles.

Gayles does not show maintaining the second node at its previously driven logic state as recited in claim 12. In the Office Action, Gayle's node 15 is considered as reading on Applicant's first node and the output of the inverter 17 is considered as reading on Applicant's second node. Since the output of the inverter 17 is always driven to the opposite state of node 15 in Gayle, its state is never maintained to its previously driven logic state but instead is always switched to the opposite state of node 15. Furthermore, Gayles does not show "driving an output node based on the states of the first and third nodes" as recited in claim 12. As shown in FIG. 2 of Gayles, the output node is driven solely by the output of the inverter 27 as controlled by node 25 (considered as reading the third node) and not by the first node 15. Applicant respectfully submits, therefore, that claim 12 is allowable over Gayles. Claims 13-17 are allowable as depending upon an allowable claim. Applicant requests withdrawal of this rejection.

Claim 12 is amended to recite that the second node is maintained at its previously driven logic state when the clock signal transitions to the first logic state from the second logic state. Although the present invention is not limited to the specific embodiments disclosed in the present Application, FIG. 2A supports this amendment. As shown in FIG. 2A, a first node "TOP" pre-charges high when the CLK signal is low (first logic state) via device P1. If the TOP node evaluates low when CLK goes high (second logic

state), then a second node "QII" is pulled high and if the TOP node instead fails to evaluate thus remaining high, then the QII node is pulled low. When the CLK signal transitions back low (first logic state), the state of the QII node is maintained and does not change in response to the CLK signal going low.

In contrast, Gayles second node (at the output of the inverter 17) always resets back low when the CLK signal goes low, so that the state of the second node in Gayles is not maintained at its previously driven logic state when the CLK signal goes back low. Applicant respectfully submits, therefore, that claim 12 is allowable over Gayles. Claims 13-17 are allowable as depending upon allowable claim 12. Applicant requests withdrawal of this rejection.

Applicant respectfully traverses the §103(a) rejection of claims 7-9 as being unpatentable over Ngo in view of Sprague.

As stated in the Office Action, Ngo does not disclose an output circuit. And as submitted above, Sprague does not show a register including an output circuit having a first input coupled to a first node, a second input coupled to a third node and an output that drives the output node high if the first or third nodes are low and that drives the output node low if the first and third nodes are both high as recited in amended claim 7. Applicant respectfully asserts that claim 7 is allowable over Ngo in view of Sprague and that claims 8-9 are allowable as depending upon allowable claim 7. Applicant request withdrawal of this rejection.

None of the amendments made herein were related to the statutory requirements of patentability, but instead were made for purposes of clarity and to remove extraneous

and/or unnecessary language. Also, none of the amendments were made for the purpose of narrowing the scope of any claim

CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the objections and rejections have been overcome and should be withdrawn. Applicant respectfully submits therefore that the present application is in a condition for allowance and reconsideration is respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

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